

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number		10550326
	Filing Date		2005-09-23
	First Named Inventor	Roger D. Chamberlain	
	Art Unit	2131	
	Examiner Name		
	Attorney Docket Number	53047-57365	

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	2	3611314	A	1971-10-05	Pritchard, Jr. et al.	
	3	3729712	A	1973-04-24	Glassman	
	4	3824375	A	1974-07-16	Gross et al.	
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9	4314356	A	1982-02-02	Scarbrough	
10	4385393	A	1983-05-24	Chaure et al.	
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5	20030093347	A1	2003-05-15	Gray	
6	20030126065	A1	2003-07-03	Eng et al.	
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	16	20050187845	A1	2005-08-25	Eklund et al.	
	17	20050187846	A1	2005-08-25	Subbu et al.	
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	27	20060020536	A1	2006-01-26	Renton et al.	
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	1	0851358	EP	A	1998-07-01	Sun Microsystems Inc		<input type="checkbox"/>
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	1	"Lucent Technologies Delivers "Payload Plus" Network Processors for Programmable, Multi-Protocol, OC-48c Processing", Lucent Technologies Press Release, downloaded from <a href="http://www.lucent.com/press/1000/0010320.meb.html">http://www.lucent.com/press/1000/0010320.meb.html</a> on March 21, 2002		<input type="checkbox"/>

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2	"Overview, Field Programmable Port Extender", January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	<input type="checkbox"/>
3	"Payload Plus™ Agere System Interface", Agere Systems Product Brief, June 2001, downloaded from Internet, January 2002	<input type="checkbox"/>
4	"The Field-Programmable Port Extender (FPX)", downloaded from <a href="http://www.arl.wustl.edu/arl/">http://www.arl.wustl.edu/arl/</a> in March 2002	<input type="checkbox"/>
5	ANONYMOUS; "Method for Allocating Computer Disk Space to a File of Known Size", IBM Technical Disclosure Bulletin, Vol. 27, No. 10B, March 1, 1985, New York	<input type="checkbox"/>
6	ARNOLD et al.; "The Splash 2 Processor and Applications"; Proceedings 1993 IEEE International Conference on Computer Design: VLSI In Computers and Processors (ICCD '93); October 3, 1993; pp 482-485; IEEE Computer Society; Cambridge, MA USA	<input type="checkbox"/>
7	BAER, JEAN-LOUP; "Computer Systems Architecture"; 1980; pp. 262-265; Computer Science Press; Potomac, Maryland	<input type="checkbox"/>
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10	BRAUN et al., "Layered Protocol Wrappers for Internet Packet Processing in Reconfigurable Hardware", Proceedings of Hot Interconnects 9 (HotI-9) Stanford, CA, August 22-24, 2001, pp. 93-98	<input type="checkbox"/>
11	CHOI et al., "Design of a Flexible Open Platform for High Performance Active Networks", Allerton Conference, Champaign, IL, 1999	<input type="checkbox"/>
12	CLOUTIER et al.; "VIP: An FPGA-Based Processor for Image Processing and Neural Networks"; Proceedings of Fifth International Conference on Microelectronics for Neural Networks; February 12, 1996; pp. 330-336; Los Alamitos, California	<input type="checkbox"/>

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13	COMPTON et al.; "Configurable Computing: A Survey of Systems and Software"; Technical Report, Northwestern University, Dept. of ECE, 1999	<input type="checkbox"/>
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23	HOLLAAR, "Hardware Systems for Text Information Retrieval", Proceedings of the Sixth Annual International ACM Sigir Conference on Research and Development in Information Retrieval; June 6-8, 1983, pp. 3-9; Baltimore, Maryland, USA	<input type="checkbox"/>



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24	International Search Report for PCT/US2001/011255; July 10, 2003	<input type="checkbox"/>
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27	KEUTZER et al., "A Survey of Programmable Platforms - Network Proc", University of California-Berkeley	<input type="checkbox"/>
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30	LOCKWOOD et al., "Hello, World: A Simple Application for the Field Programmable Port Extender (FPX)", Washington University, Department of Computer Science, Technical Report WUCS-00-12, July 11, 2000	<input type="checkbox"/>
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33	LOCKWOOD, J., "An Open Platform for Development of Network Processing Modules in Reprogrammable Hardware", IEC DesignCon 2001, Santa Clara, CA, January 2001, Paper WB-19	<input type="checkbox"/>
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35	LOCKWOOD, J., "Evolvable Internet Hardware Platforms", NASA/DoD Workshop on Evolvable Hardware (EHW'01), Long Beach, CA, July 12-14, 2001, pp. 271-279	<input type="checkbox"/>
36	LOCKWOOD, J., "Hardware Laboratory Configuration", Field Programmable Port Extender: January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	<input type="checkbox"/>
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41	LOCKWOOD, J., "Simulation of the Hello World Application for the Field-Programmable Port Extender (FPX)", Washington University, Applied Research Lab, Spring 2001 Gigabits Kits Workshop	<input type="checkbox"/>
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43	MOSCOLA et al., "FPGrep and FPSed: Regular Expression Search and Substitution for Packet Streaming in Field Programmable Hardware", unpublished, pp. 1-19.	<input type="checkbox"/>
44	NAVARRO, "A Guided Tour to Approximate String Matching", ACM Computing Surveys, Vol. 33, No. 1, March 2001, pp. 31-88.	<input type="checkbox"/>
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	47	PRAMANIK et al.; "A Hardware Pattern Matching Algorithm on a Dataflow"; Computer Journal; July 1, 1985; pp. 264-269; Vol. 28, No. 3; Oxford University Press, Surrey, Great Britain	<input type="checkbox"/>
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